A dual mode PWM based 4T pixel CMOS image sensor for higher dynamic range and low power imaging applications

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***Abstract*—This paper presents a 4T pixel CMOS image sensor suitable for indoor and outdoor low-power imaging applications. The sensor has two operational modes: low noise (LN) and high dynamic range (HDR). The pixel operates based on a PWM technique and is implemented using a single NMOS as a comparator. In LN mode, the pixel is operated similarly to a 4T pixel, and in HDR mode, it is operated as a 3T. The prototype chip was fabricated in the 180 nm 1P6M CIS process and has a pixel array 128x128. It achieves a noise of 5 e^-_{RMS} in LN mode and a dynamic range of more than 100 dB in HDR mode.**

***Keywords*—** CMOS Image Sensors(CIS), Low Noise (LN), High Dynamic Range (HDR), Pulse Width Modulation (PMW)

I. Introduction

Emerging applications in consumer imaging like augmented reality (AR), virtual reality (VR), wireless sensor nodes, Internet-of-Things (IoT), and remote surveillance require continuous imaging to track objects and extract information in real time. The image sensors for such applications require always-ON imaging and a good dynamic range for reliable object detection [1,3,5]. The existing solutions use conventional 3T pixel with pulse width modulation (PWM) readout architecture to reduce power consumption while achieving high dynamic range. The PWM based imaging sensors encode light intensity into time-domain pulse-width signals. This enables improved performance of imaging sensors in energy-constrained applications.

The pixel front-end readout circuit in these topologies restricts their use in low-light imaging due to higher readout noise [2,4]. The earlier approaches with 4T pixel and PPD (pinned photo-diode) show low readout noise but fail to provide a very high dynamic range [1]. On the contrary, pixel architectures with simple photodiodes achieve a high dynamic range with the PMW readout technique but have higher readout noise [2, 4]. This limits the use of the sensor to only particular applications. This work presents a novel pixel architecture using a PPD and an in-pixel comparator to generate a PWM as the pixel output in the column. The designed pixel is capable of delivering low noise and a high dynamic range mode sensing while consuming very low power.

The rest of the paper is organized as follows: section II presents an overview of low power CMOS image sensor. Section III presents the measurement results of the fabricated sensor. Section IV concludes the paper.

II. Overview of low power CIS

Figure 1 shows the four transistor pixel circuit and the column readout circuit for the proposed low-power CIS.

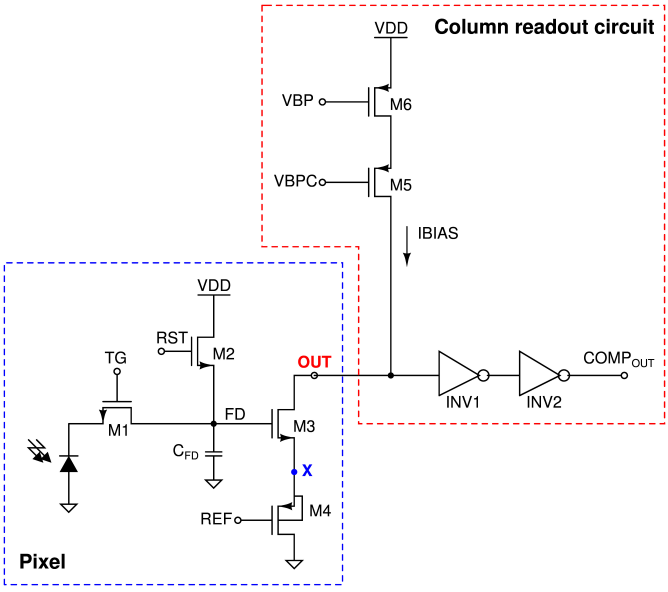

Figure 1: Proposed 4T pixel with column readout circuit

The pixel consists of a pinned photodiode (PPD), a reset gate (RST), a transfer gate (TG), an N-MOSFET as comparator and an P-MOSFET as an source follower (SF). The column readout circuit contains a current source shared with column pixels and a pair of inverters as digital drivers. The column output $COMP_{OUT}$ is applied at the column digital memory to latch data bits from a digital counter. The pixel array is readout in rolling shutter manner and is operated with row decoder. Digital data from column memory is readout sequentially by using column decoder circuit.

A. Voltage to Time pulse conversion with PWM

Figure 2 shows the timing diagram for pixel operation and readout with the PWM technique. Voltage-to-time pulse conversion is implemented inside the pixel with a single NMOS as a comparator. A positive slope ramp is applied at the gate of PMOS, resulting in a voltage ramp at the source of NMOS (X) with a shift of V_{SG} of PMOS. A 12-bit digital gray counter is used operating at 1 MHz. At the start of the ramp, the NMOS gets biased in the triode region, pulling the OUT node, close to the source voltage. With time, the source node voltage of NMOS increases, decreasing its V_{GS}. This gradually increases the drain to source resistance of NMOS and thus voltage across it. The NMOS gradually changes the operating region from triode to sub-threshold. When the V_{GS} crosses the threshold voltage of NMOS, it gets biased as a common-gate amplifier, providing higher gain to the ramp voltage input.

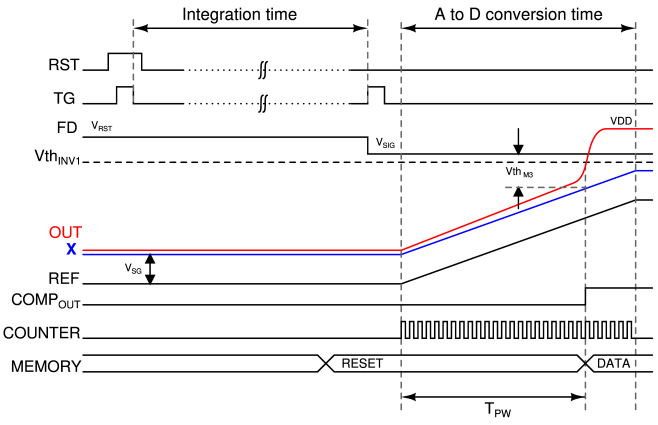

Figure 2: Timing diagram for Voltage to Time pulse conversion

The first inverter is sized to have a higher threshold voltage. When the OUT node crosses the inverter threshold, $COMP_{OUT}$ transitions from low to high. This comparator trigger latches the 12-bit counter data into the column memory. The memory data is read out sequentially before the start of the next A-to-D conversion. The obtained time pulse width is inversely proportional to the photoelectrons.

The readout is then progressed to the next row, and the ramp is applied to the row being read. The pixels of other rows are cut off by applying 3.3 V to the gate of PMOS.

B. Low Noise (LN) mode of operation

The reset switch noise at the FD node is dominant. As the analog voltage signal is converted into a time pulse inside the pixel, conventional analog CDS cannot be used. The noise cancellation is done in the digital domain. The FD node is reset, and digitized using a small ramp. The digital data is read and stored off-chip. After the charges are transferred from PPD to FD node, the signal is digitized again using a full ramp. The digital output is again read out and subtracted from the reset data off-chip. This digital CDS (Correlated Double Sampling) cancels out the reset noise. A gain of 10 in the comparator signal path further reduces the input refereed noise. The bandwidth reduction at the pixel output to a few kHz further lowers the thermal noise contribution. A readout noise of 5 e^-_{RMS} is achieved with this pixel.

C. High Dynamic Range (HDR) mode of operation

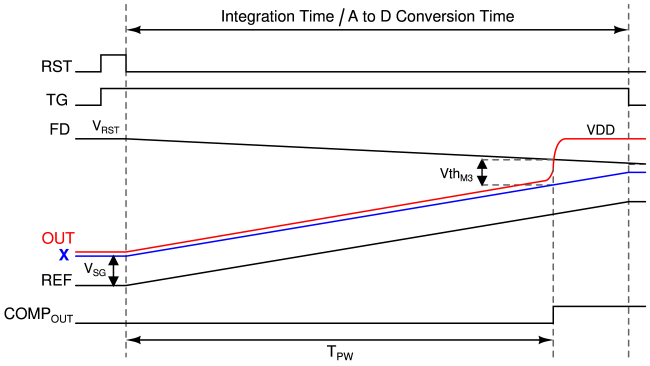

Figure 3: Timing diagram in HDR mode

In the HDR mode of operation, voltage-to-time pulse conversion is done simultaneously with photo-electron integration, as shown in Figure 3. After resetting the PPD and FD node, TG is made ON along with the start of integration time. This causes the photoelectrons to flow towards the FD node with higher potential. The continuous flow of electrons discharges the FD node voltage at a rate proportional to the light received onto the photodiode. The reference voltage for comparator operation becomes non-linear compared to the LN mode readout. The output pulse width becomes a hyperbolic function of the amount of light received. This increases the dynamic range significantly compared to the LN mode of operation [4]. The measured dynamic range for an integration time of 30 milli-seconds is more than 100 dB. As the pixel is operated similarly to the 3T pixel, the reset switch noise at the FD node cannot be canceled.

III. Measurement results

Figure 4 shows the photograph of the microchip die with a size of 2.64 mm x 2.06 mm. The sensor is fabricated in the TSMC 180 nm 1P6M CIS process. It works on 3.3 V analog and 1.8 V digital power supply. The pixel pitch is 5.6 μm x 5.6 μm and a resolution of 128 x 128 pixels.

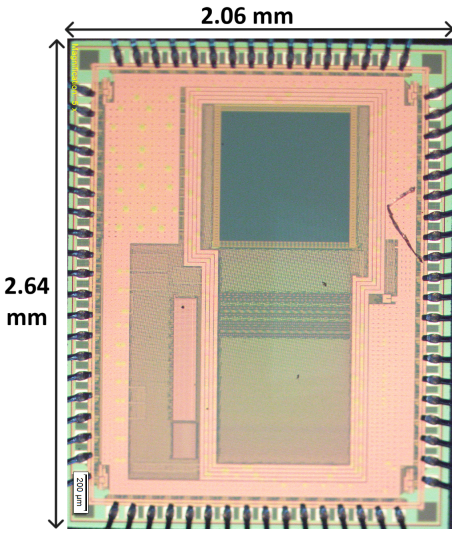

Figure 4: Microchip photograph of sensor

Figure 5 shows the measurement setup. Corresponding images have been captured using Pleora iPORT CL-U3 frame grabber.

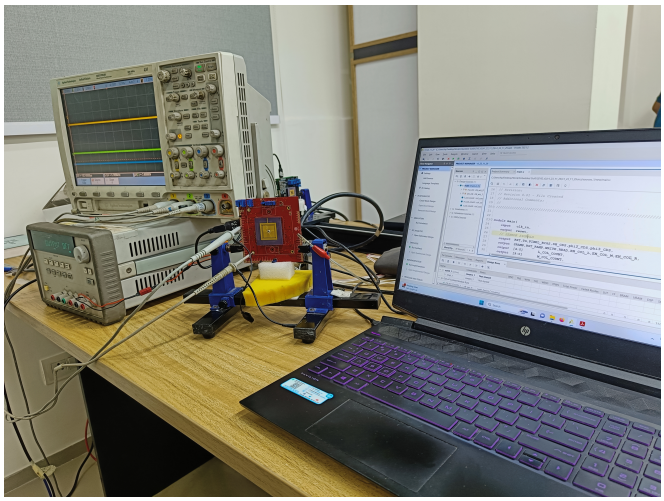

Figure 5: Measurement Setup

Figures 6 and 7 show the measured photoresponse in LN and HDR mode. Compared to the DR of around 60 dB in LN mode, HDR mode achieves a DR of more than 100 dB. The readout noise of 5 e^-_{RMS} in LN mode and of 25 e^-_{RMS} in HDR mode is achieved with the proposed pixel architecture. The CIS consumes a power of 3.262 mW at a maximum of 80 FPS in LN mode, while it consumes around 2.02 mW at 19 FPS in HDR mode.

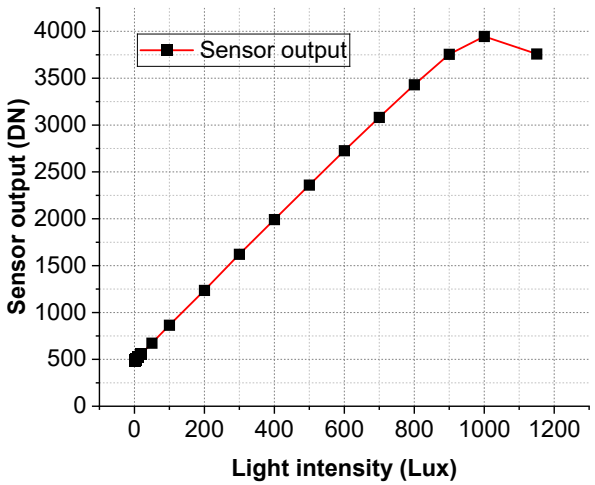

Figure 6: Photoresponse in LN mode

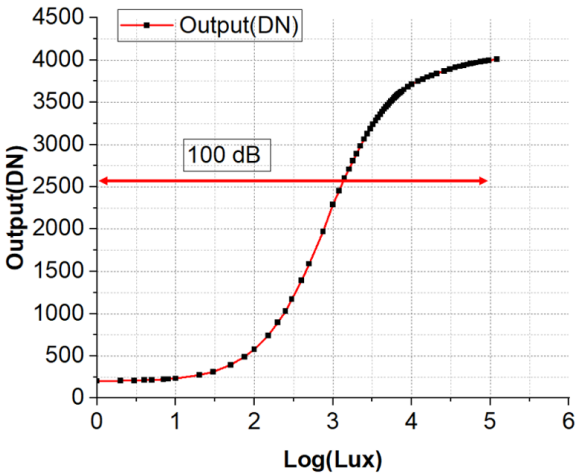

Figure 7: Photoresponse in HDR mode

Figure 8 shows the dark frame subtracted image without reset noise cancellation. A shiny object was illuminated with a 10 klux DC light source in the dark background to check HDR mode. Figure 9 shows that the saturated features of the object in LN mode are clearly visible in the HDR mode. Table I shows the measured specifications of CIS.

Table I: Sensor specifications

Technology	180 nm CIS
Pixel type	4T APS with PPD
Array size	128 × 128
Pixel pitch (µm)	5.6
Supply voltage (V)	3.3/1.8
Dynamic range (dB)	60 (LN) / >100 (HDR)
Power consumption (mW)	3.262 @ 80 FPS (LN) / 2.02 @ 19 FPS (HDR)
Noise (e^-_{RMS})	5 (LN) / 25 (HDR)

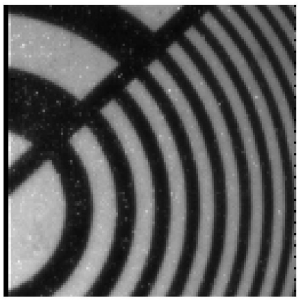

Figure 8: Dark frame corrected image without reset noise cancellation

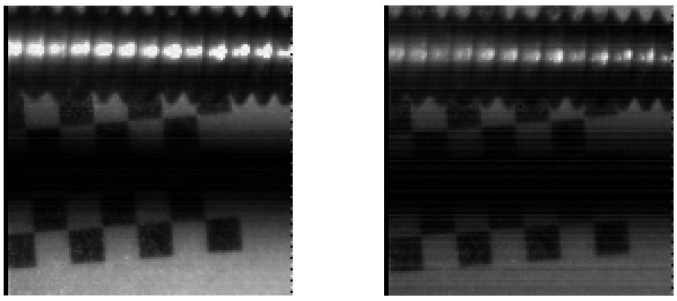

Figure 9: Raw image without and with HDR mode

IV. Conclusion

A CMOS image sensor with dual operational modes (LN and HDR) making it suitable for indoor and outdoor low-power imaging applications is demonstrated. The incident light intensity is converted to a digital pulse width via the in-pixel comparator that triggers when integrated photodiode voltage matches a global ramp signal. A prototype CIS of a 128 x 128 pixel array has been designed and fabricated in the TSMC 180 nm 1P6M CIS process. The pixel is operated similarly to a conventional 4T pixel to get a low noise and as a 3T pixel to achieve a dynamic range of around 100 dB. Pixel achieves a noise level of 5 e^-_{RMS} in LN mode and 25 e^-_{RMS} in HDR mode. The CIS consumes a power of 3.262 mW in LN mode at 80 FPS and 2.02 mW in HDR mode at 19 FPS. Power optimization can be done further with low-power periphery circuits.

References

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